Universal High Brightness LED Driver Controller

Features

- **Buck system efficiency：>90%**
- **Open loop peak current controller**
- **Internal 8~450V linear regulator**
- **Constant Current LED Driver**
- **LED string from one to hundreds of diodes**
- **Support linear and PWM dimming interface**
- **Requires few external components**
- **8 Lead SOIC Packages**
- **RoHS Compliant and 100% Lead (Pb)-Free and Green (Halogen Free with Commercial Standard)**
- **Constant off time function when duty cycle over 50%**

Applications

- LED driver applications
- RGB backlighting LED driver
- General purpose constant current source
- Chargers
- Non-isolation LED bulb

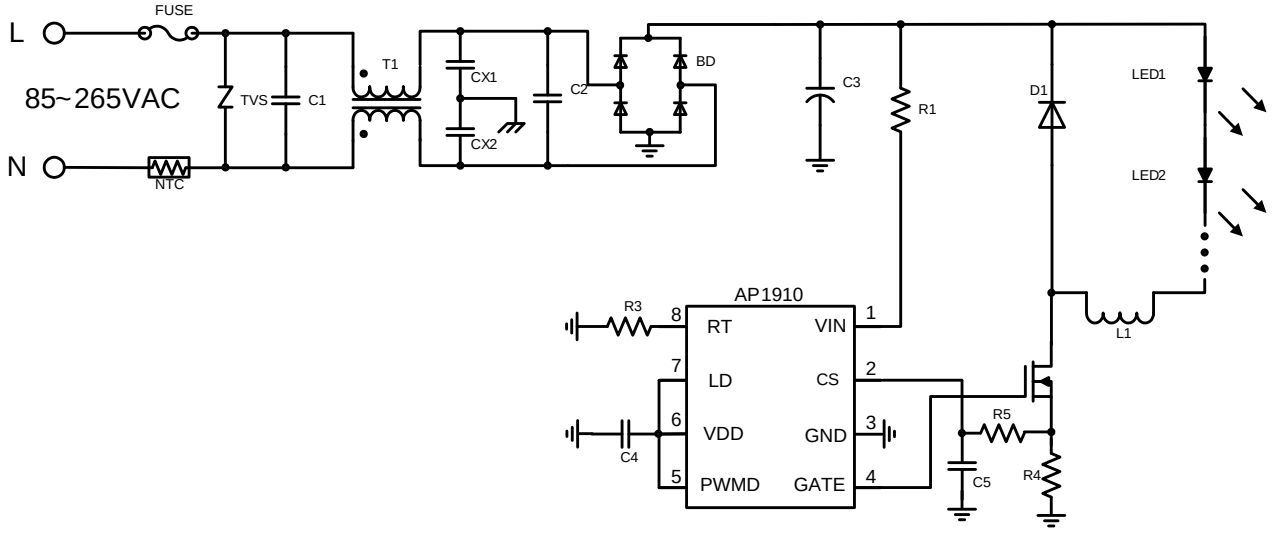
General Description

The AP1910 is a high-efficiency LED driver control IC. It drives LEDs with constant current and uses fewer components. The AP1910 is an open loop, current mode control IC. It can be programmed to operate in either a constant frequency or constant off-time mode. It includes an 8~450V linear regulator which allows it to work in wide input voltage range without external low voltage power supply. The AP1910 is recommended in buck LED drivers applications, LED luminance can be easily adjusted by AP1910's 0~100% PWM dimming and 0~245mV linear dimming functions.

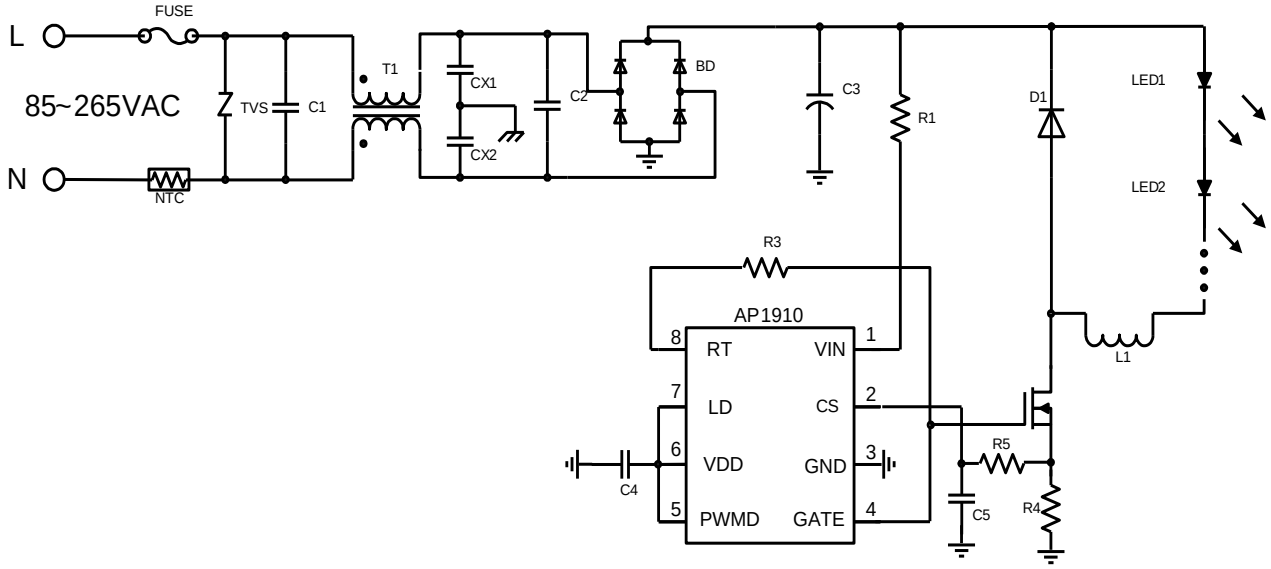
The AP1910 is suitable for buck LED drivers. The system has excellent stable response because of open loop current mode control. The controller achieves good output current regulation and need no compensation.

Typical Application Circuit

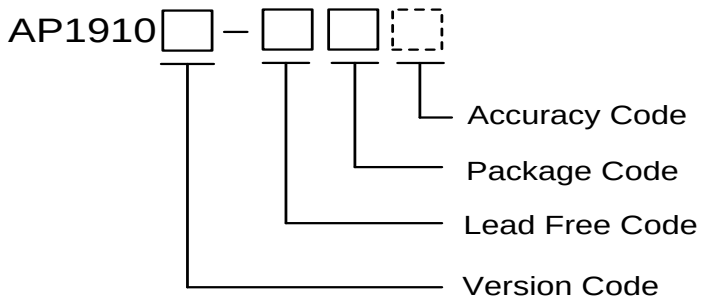
(A) Constant Frequency mode



(B) Constant Off-time mode



Ordering Information



Version Code：

A：First Issue **B**：Second Issue **C…**

Lead Free Code：

P：Commercial Standard, Lead (Pb) Free and Phosphorous (P) Free Package

G：Green (Halogen Free with Commercial Standard)

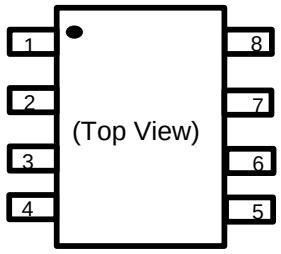
Package Code：

A：SOIC-8

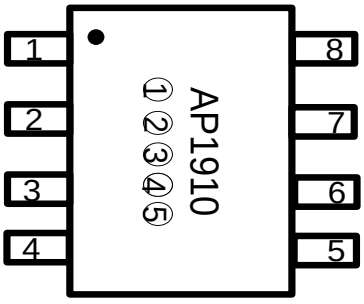
Accuracy Code：

1 = 4% Accuracy **2 =** 2% Accuracy

Pin Description

Part No.	Pin	Symbol	Pin Description
 SOIC-8	1	VIN	Input voltage 8~450V DC
	2	CS	Sense LED string current
	3	GND	Ground Pin
	4	GATE	Driver external N-Mosfet
	5	PWMD	PWM dimming input from 0%~100%
	6	VDD	Internal power source input for logic circuit
	7	LD	Linear dimming input
	8	RT	Frequency controlled by external resistor. Constant off-time: resistor connected to GATE Constant frequency: resistor connected to GND

Package Marking Information



SOIC-8
(Top View)

① **Represents Version Code**

Mark	Description
①	**Version Code**

② **Represents Accuracy**

Mark	Description
1	**1=4% accuracy**
2	**2=2% accuracy**

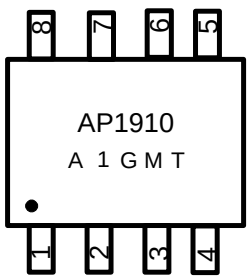
③ **Represents Products Lead Free type**

Mark	Description
G	**Green (Halogen Free)**

④、⑤ **Represents Products Series**

Description
date code

Example：



Part No.:AP1910A-GA
Year Code:2012
Week Code: 22th week
Green (Halogen Free)

Absolute Maximum Ratings

Parameter (PIN)		Symbol	Ratings	Units
VIN to GND		--	500	V
VDD, LD, PWMD, GATE to GND		--	36	V
CS, RT, to GND		--	7	V
Junction Temperature		T_J	+150	°C
Thermal Resistance	SOIC-8	θ_{JA}	130	°C/W
Power Dissipation	SOIC-8	P_D	630	mW
Operating Ambient Temperature		T_{OPR}	-40 ~ +85	°C
Storage Temperature		T_{STG}	-55 ~ +150	°C
Lead Temperature (soldering, 10sec)		--	+260	°C

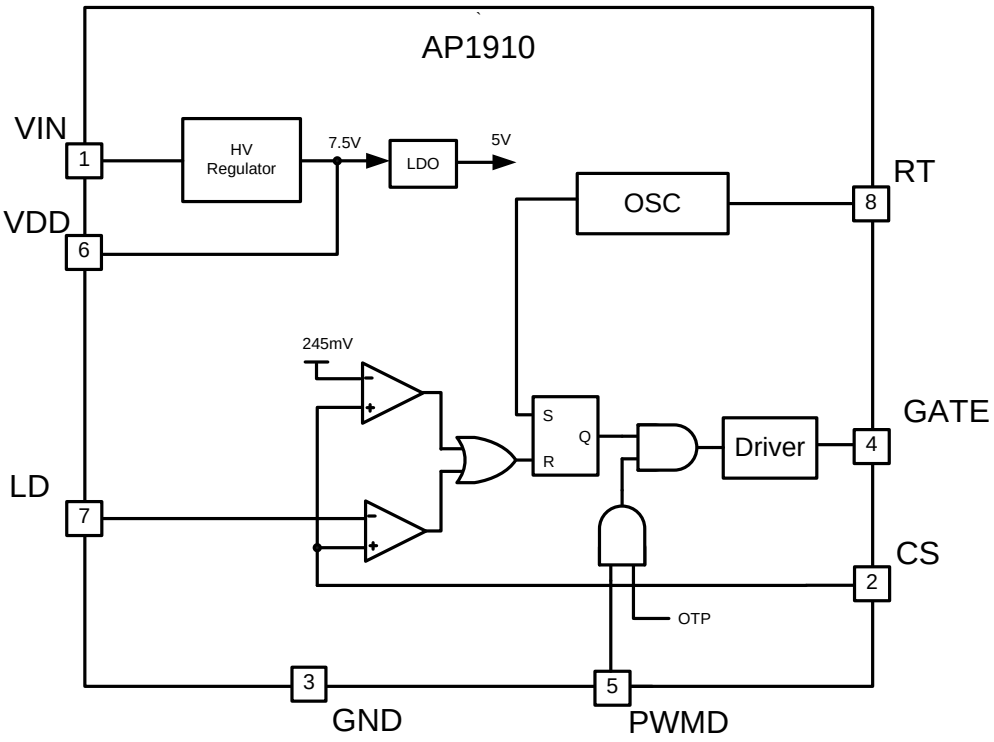
Note：

* The power dissipation values are based on the condition that junction temperature T_J and ambient temperature T_A difference is 100°C.

* Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and function operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum -rated conditions for extended periods may affect device reliability.

*Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the recommended operating conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

AP1910 Function Block Diagram



Electrical Characteristics

(T_A=25℃, unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{INDC}	Input DC supply voltage range	Line Voltage or DC input voltage	8		450	V
I_{INSD}	Shut-Down mode supply current	PWM_D to GND, VIN=8V		0.1	0.2	mA
V_{DD}	Internal regulated voltage	V_{IN}=8~450V	6.7	7.5	8	V
UVLO	VDD under voltage lockout threshold	V_{DD} rising	5.5	6	6.5	V
ΔUVLO	UVLO hysteresis	V_{DD} falling		500		mV
$V_{EN(hi)}$	PWMD input high level	V_{IN}=8~450V	2.0			V
$V_{EN(lo)}$	PWMD input low level	V_{IN}=8~450V			0.8	V
V_{CS-TH}	Current sense pull-in threshold voltage	V_{IN}=8~450V，T_A=25°C	235	245	255	mV
V_{LD}	Linear dimming pin voltage range	V_{IN}=8~450	0		250	mV
T_{BLANK}	Current sense blanking time	T_A=25 °C, V_{LD} = V_{DD}, V_{CS} = V_{CS-TH} + 50mV after T_{BLANK}	250	500	650	ns
F_{OSC}	Oscillator frequency	R_{OSC} = 1MΩ (Connect to RT and GND)		21		KHz
		R_{OSC} = 200KΩ (Connect to RT and GND)		93		KHz
T_{OFF}	Constant off-time	R_{OFF} = 1MΩ (Connect to RT and GATE)		54		us
		R_{OFF} = 200KΩ (Connect to RT and GATE)		13		us
D_{MAX}	Maximum duty cycle	HV floating			95	%
I_{SOURCE}	GATE sourcing current	V_{GATE}=0V, V_{DD}=7.5V	165			mA
I_{SINK}	GATE sinking current	V_{GATE}= V_{DD}, V_{DD}=7.5V	165			mA
t_R	GATE rising time	C_{GATE}= 500pF, V_{DD}=7.5V		50	150	ns
t_F	GATE falling time	C_{GATE}= 500pF, V_{DD}=7.5V		50	150	ns
T_{TST}	Thermal Shutdown Temperature			155		°C
T_{TSH}	Thermal Shutdown Hysteresis			40		°C

Note : The suggest Qg of NMOS around 6.5 nC(Typ.),it can improve efficiency.

Detail Description

The AP1910 is a low-cost buck, boost or buck-boost converter controller specifically designed for driving multi LED strings or arrays. It can be operated from either universal 90~264Vac or DC voltage between 20 and 450Vdc. The AP1910 can also drive multiple strings of High-Brightness (HB) LEDs. The AP1910 could regulate constant current to ensure controlled brightness and spectrum of the LEDs. Constant current driving method can also improve LEDs lifetime. The AP1910 supports soft start function to reduce inrush current. It can add resistor from VDD to LD pin to generate 1~5uA current and charge LD capacitor. The voltage level will rising with slop and correspond to CS pin current limit level. The IC has feed-forward compensation by setting suitable resistor in CS pin to keep LED string constant current when line voltage variation.

The AP1910 include an internal high voltage linear regulator to generate fix VDD voltage supply to IC internal logic circuit.

LED Driver Operation

The AP1910 controls all basic types of converters, non-isolated, operating in continuous or discontinuous conduction mode. N-MOSFET is turned on when PIN GATE is high, and the input energy is delivered to LED driver and stored in an inductor. The energy is stored in the inductor free wheeling itself through the string of LEDs when power switch off.

When the VDD pin voltage exceeds the UVLO threshold, the internal power switch is enabled. The output current is controlled by mean of limiting peak current of CS pin. The peak current limit level is set by LD pin of the AP1910.

The AP1910 using Buck topology needs to design the duty cycle below 50% to prevent unregulated Gate output pulse. It can apply resistor between RT and Gate pin. That is constant off time function when duty over 50%.

Supply Current

A current of 0.2mA is needed after start up the AP1910 controller. This current is generated from internal HV regulator circuit. The AP1910 without using bulky startup resistors typically required in the offline applications. Moreover, in many applications using AP1910 can be continuously powered because of its internal linear regulator that provides a regulated voltage of 7.5V for internal circuits. The IC power consumption is very low when high line input voltage because of low operating current.

Current Sense

The current sense input of the AP1910 goes to the non-inverting inputs of two comparators. The inverting terminal of one comparator is tied to an internal 245mV reference whereas the inverting terminal of the other comparator is connected to the LD pin. The outputs of both these comparators are fed into an or gate and the output of the or gate is fed into the reset pin of the flip-flop. Thus the comparator which has the lowest voltage at the inverting terminal determines when the GATE output is turned off.

The outputs of the comparators also include a 500ns blanking time due to the turn on spike current. Some solution will add RC filter to prevent this situation.

Linear Dimming

The AP1910 has two type dimming functions. The Linear dimming is setting LD pin voltage level to adjust current limit.

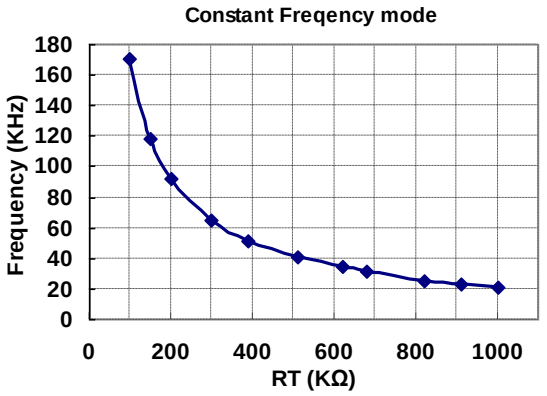
PWM Dimming

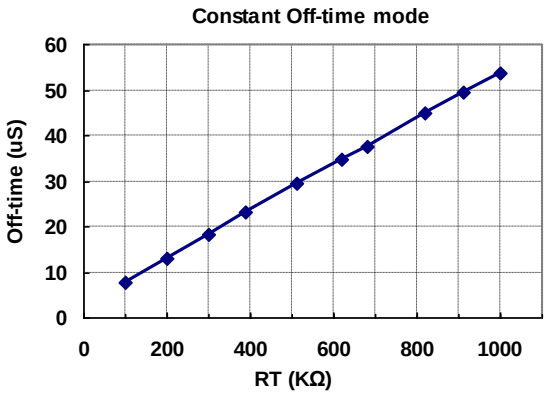
PWM dimming can be achieved by driving the PWMD pin with a low frequency square wave signal. When the PWM signal is zero, the GATE driver is turned off and when the PWMD signal if high, the GATE driver is enabled. On the other hand, the GATE driver is disabled.

Detail Description (Continued)

Operating Frequency

The operating frequency of AP1910 can be set by the external resistor connected to RT pin. Connecting the resistor from RT to GND for constant frequency operation mode or RT to GATE for constant off-time operation mode. Following diagram is the reference data for setting switching frequency.





Inductor Design

Referring to the typical application circuit below the value can be calculated from the desired peak-to-peak LED ripple current in the inductor.

Typically, such ripple current is selected to be 30% of the nominal LED current in the example given here, the nominal current I_{LED} is 350mA. The next step is determining the total voltage drop across the LED string. For example, when the string consists of 10 HB LEDs and each diode has forward voltage drop of 3V at its nominal current. The total LEDs voltage V_{LEDS} is 30V.

Knowing the nominal rectified input line voltage V_{IN}=120V*1.414=170V. The switching duty ratio can be determined as:

$$D = V_{LEDS} / V_{IN} = 30/170 = 0.176$$

Then, given the switching frequency 50KHz. The required on time of the MOSFET transistor can be calculated:

$$T_{ON} = D / f_{OSC} = 3.52\mu s, \quad T_{OFF} = 16.48\mu s$$

The required value of the inductor is given by:

$$\frac{V_{IN} - V_{LED}}{L} * T_{ON} = 30\% * I_{LED}$$

$$L = (V_{IN} - V_{LED}) * T_{ON} / (0.3 * I_{LED}) = 4.69mH$$

Input Bulk Capacitor

An input filter capacitor should be designed to hold the rectified AC voltage above twice the LED string voltage throughout the AC line cycle.

Assuming 15% relative voltage ripple across the capacitor, a simplified formula for the minimum value of the bulk input capacitor is given by:

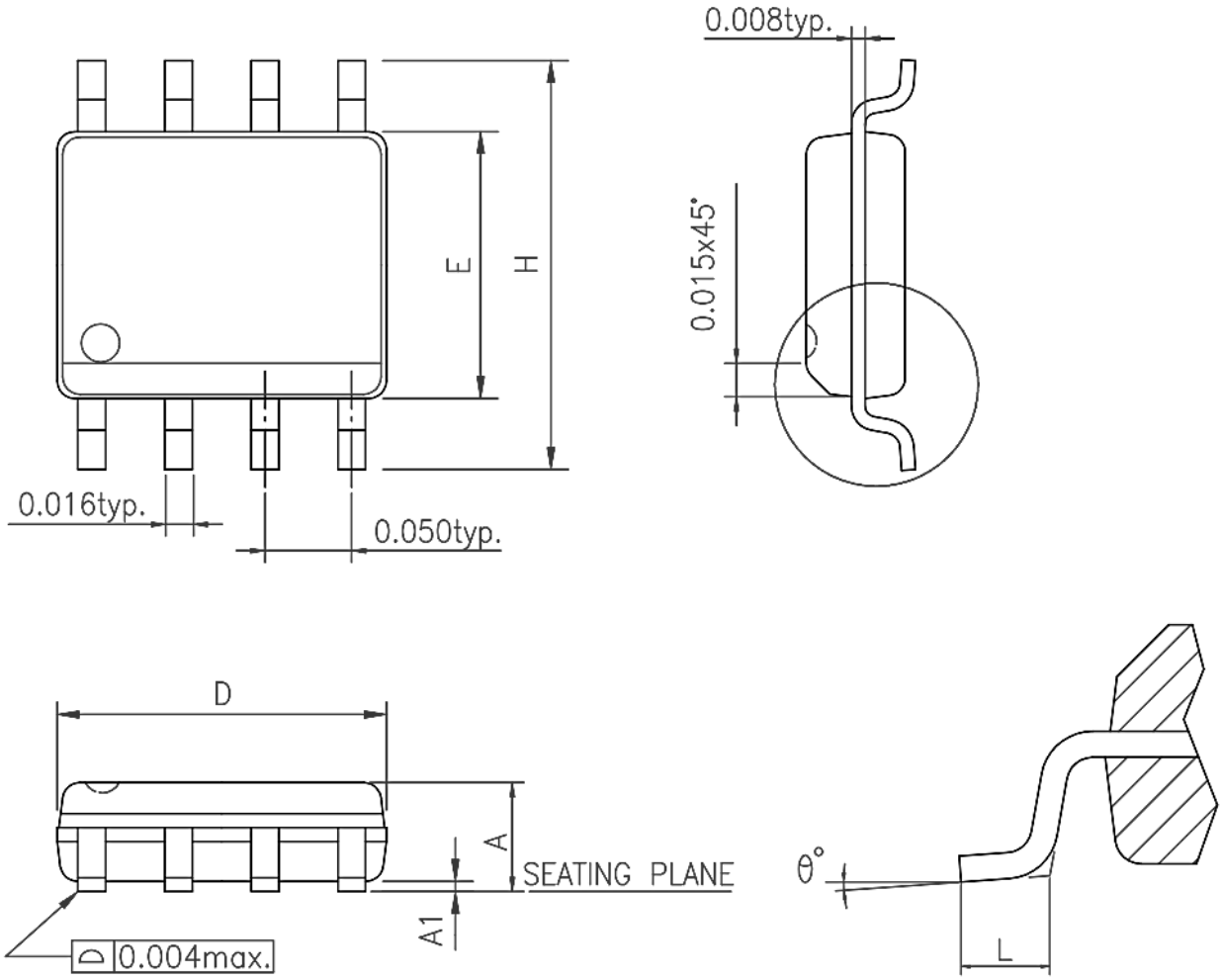
$$I_{LED} * 30\% * V_{LED} = \frac{1}{2} C_{MIN} V_{IN}^2$$

$$C_{MIN} = I_{LED} * 0.06 * V_{LED} / V_{IN}^2 = 22\mu F$$

A passive PFC circuit at the input requires using two series connected capacitors at the place of calculated C_{MIN}. Each of these identical capacitors should be rate for 0.5 of the input voltage and have twice as much capacitance.

Package Outline

SOIC-8



SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AA
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Classification Reflow Profiles

Profile Feature	Pb-Free / Green Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	217°C 60-150 seconds
Peak/Classification Temperature (Tp)	See table 1
Time within 5°C of actual Peak Temperature (tp)	20-40 seconds
Ramp-down Rate	6°C/second max
Time 25°C to Peak Temperature	8 minutes max

Notes：

1) All temperatures refer to topside of the package.
2) Measured on the body surface.

Classification Reflow Profiles (Continued)

Table 1. Pb-free / Green Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≧2000
<2.5 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6-2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≧2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*

Notes：

* Tolerance: The device manufacturer/supplier shall assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.

Appendix

Date Code Rule

Year	Week	Day-From	Day-End	Date-Code
2012	1	2012/1/1	2012/1/7	LV
2012	2	2012/1/8	2012/1/14	LW
2012	3	2012/1/15	2012/1/21	LX
2012	4	2012/1/22	2012/1/28	LY
2012	5	2012/1/29	2012/2/4	MA
2012	6	2012/2/5	2012/2/11	MB
2012	7	2012/2/12	2012/2/18	MC
2012	8	2012/2/19	2012/2/25	MD
2012	9	2012/2/26	2012/3/3	ME
2012	10	2012/3/4	2012/3/10	MF
2012	11	2012/3/11	2012/3/17	MG
2012	12	2012/3/18	2012/3/24	MH
2012	13	2012/3/25	2012/3/31	MJ
2012	14	2012/4/1	2012/4/7	MK
2012	15	2012/4/8	2012/4/14	ML
2012	16	2012/4/15	2012/4/21	MM
2012	17	2012/4/22	2012/4/28	MN
2012	18	2012/4/29	2012/5/5	MP
2012	19	2012/5/6	2012/5/12	MQ
2012	20	2012/5/13	2012/5/19	MR
2012	21	2012/5/20	2012/5/26	MS
2012	22	2012/5/27	2012/6/2	MT
2012	23	2012/6/3	2012/6/9	MU
2012	24	2012/6/10	2012/6/16	MV
2012	25	2012/6/17	2012/6/23	MW
2012	26	2012/6/24	2012/6/30	MX
2012	27	2012/7/1	2012/7/7	MY
2012	28	2012/7/8	2012/7/14	NA
2012	29	2012/7/15	2012/7/21	NB
2012	30	2012/7/22	2012/7/28	NC
2012	31	2012/7/29	2012/8/4	ND
2012	32	2012/8/5	2012/8/11	NE
2012	33	2012/8/12	2012/8/18	NF
2012	34	2012/8/19	2012/8/25	NG
2012	35	2012/8/26	2012/9/1	NH
2012	36	2012/9/2	2012/9/8	NJ
2012	37	2012/9/9	2012/9/15	NK
2012	38	2012/9/16	2012/9/22	NL
2012	39	2012/9/23	2012/9/29	NM
2012	40	2012/9/30	2012/10/6	NN
2012	41	2012/10/7	2012/10/13	NP
2012	42	2012/10/14	2012/10/20	NQ
2012	43	2012/10/21	2012/10/27	NR
2012	44	2012/10/28	2012/11/3	NS
2012	45	2012/11/4	2012/11/10	NT
2012	46	2012/11/11	2012/11/17	NU
2012	47	2012/11/18	2012/11/24	NV
2012	48	2012/11/25	2012/12/1	NW
2012	49	2012/12/2	2012/12/8	NX
2012	50	2012/12/9	2012/12/15	NY
2012	51	2012/12/16	2012/12/22	PA
2012	52	2012/12/23	2012/12/29	PB

Appendix (Con't)

Date Code Rule

Year	Week	Day-From	Day-End	Date-Code
2013	1	2012/12/30	2013/1/5	PC
2013	2	2013/1/6	2013/1/12	PD
2013	3	2013/1/13	2013/1/19	PE
2013	4	2013/1/20	2013/1/26	PF
2013	5	2013/1/27	2013/2/2	PG
2013	6	2013/2/3	2013/2/9	PH
2013	7	2013/2/10	2013/2/16	PJ
2013	8	2013/2/17	2013/2/23	PK
2013	9	2013/2/24	2013/3/2	PL
2013	10	2013/3/3	2013/3/9	PM
2013	11	2013/3/10	2013/3/16	PN
2013	12	2013/3/17	2013/3/23	PP
2013	13	2013/3/24	2013/3/30	PQ
2013	14	2013/3/31	2013/4/6	PR
2013	15	2013/4/7	2013/4/13	PS
2013	16	2013/4/14	2013/4/20	PT
2013	17	2013/4/21	2013/4/27	PU
2013	18	2013/4/28	2013/5/4	PV
2013	19	2013/5/5	2013/5/11	PW
2013	20	2013/5/12	2013/5/18	PX
2013	21	2013/5/19	2013/5/25	PY
2013	22	2013/5/26	2013/6/1	QA
2013	23	2013/6/2	2013/6/8	QB
2013	24	2013/6/9	2013/6/15	QC
2013	25	2013/6/16	2013/6/22	QD
2013	26	2013/6/23	2013/6/29	QE
2013	27	2013/6/30	2013/7/6	QF
2013	28	2013/7/7	2013/7/13	QG
2013	29	2013/7/14	2013/7/20	QH
2013	30	2013/7/21	2013/7/27	QJ
2013	31	2013/7/28	2013/8/3	QK
2013	32	2013/8/4	2013/8/10	QL
2013	33	2013/8/11	2013/8/17	QM
2013	34	2013/8/18	2013/8/24	QN
2013	35	2013/8/25	2013/8/31	QP
2013	36	2013/9/1	2013/9/7	QQ
2013	37	2013/9/8	2013/9/14	QR
2013	38	2013/9/15	2013/9/21	QS
2013	39	2013/9/22	2013/9/28	QT
2013	40	2013/9/29	2013/10/5	QU
2013	41	2013/10/6	2013/10/12	QV
2013	42	2013/10/13	2013/10/19	QW
2013	43	2013/10/20	2013/10/26	QX
2013	44	2013/10/27	2013/11/2	QY
2013	45	2013/11/3	2013/11/9	RA
2013	46	2013/11/10	2013/11/16	RB
2013	47	2013/11/17	2013/11/23	RC
2013	48	2013/11/24	2013/11/30	RD
2013	49	2013/12/1	2013/12/7	RE
2013	50	2013/12/8	2013/12/14	RF
2013	51	2013/12/15	2013/12/21	RG
2013	52	2013/12/22	2013/12/28	RH
2013	53	2013/12/29	2014/1/4	RJ